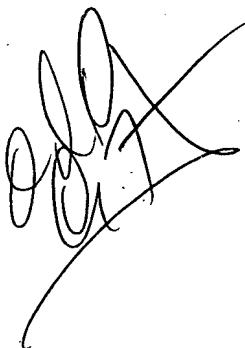


CLAIMS

1. A MOS transistor with a controlled threshold voltage, comprising a SOI which includes a substrate composed of a semi-conducting material, a single crystal layer composed of a semi-conducting material and an insulating layer interposed between said substrate and said single crystal layer,
said single crystal layer being formed therein with a source region, a drain region and a surrounded region surrounded by said source region and said drain region,
said surrounded region including a depletion layer having a composition surface which is in contact with said insulating layer,
said MOS transistor comprising an EIB-MOS transistor of which said substrate is adapted to be applied with a voltage of a first polarity for inducing charges of a second polarity over said composition surface of the surrounded region.
- 10 2. The MOS transistor according to claim 1, wherein said EIB-MOS transistor comprises an EIB-DTMOS transistor.
- 15 3. The MOS transistor according to claim 2, wherein said EIB-DTMOS transistor comprises an accumulation mode EIB-DTMOS transistor having a channel which is doped with impurities so that said channel has the same conductive type as that of carriers introduced into said channel.
- 20 4. The MOS transistor according to claim 1, wherein said EIB-MOS transistor comprises an EIB-VMOS transistor.
5. The MOS transistor according to claim 1, included in a CMOS circuit as one of pair of EIB-MOS transistors.
- 25 6. A method of controlling a threshold voltage of a MOS transistor with a controlled threshold voltage, said MOS transistor being an EIB-MOS transistor and comprising a SOI which includes a substrate composed of a semi-conducting material, a single crystal layer composed of a semi-

conducting material and an insulating layer interposed between said substrate and said single crystal layer, said single crystal layer being formed therein with a source region, a drain region and a surrounded region surrounded by said source region and said drain region, said surrounded region including a
5 depletion layer having a composition surface which is in contact with said insulating layer, wherein said method comprises the step of applying a voltage of a first polarity to said substrate for inducing charges of a second polarity over said composite surface of the surrounded region.

A handwritten signature in black ink, appearing to read "John S. Smith".

00000000000000000000000000000000